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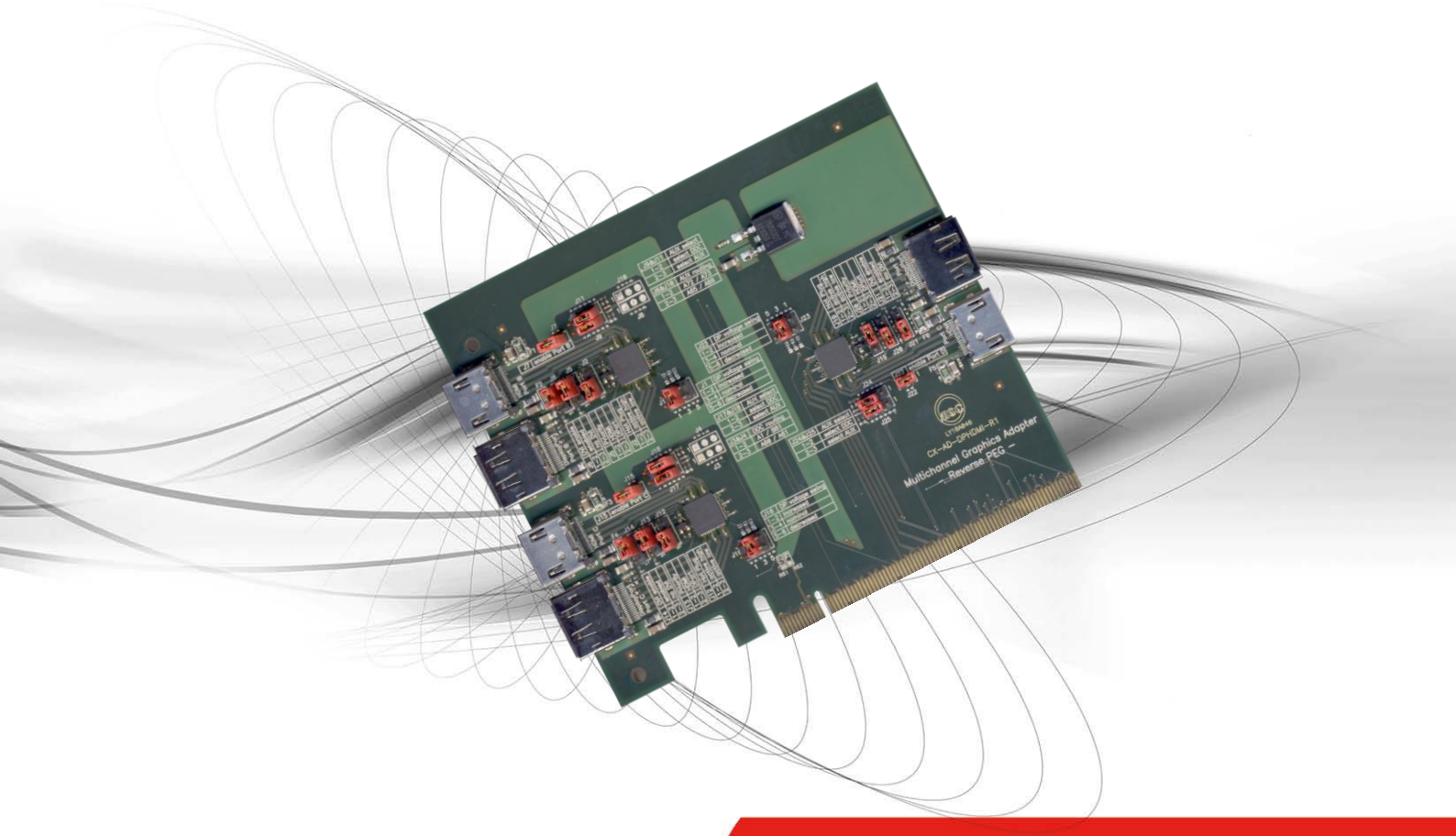

Engineering Leadership

User Manual Rev. 0.2

MSC CX-AD-DPHDMI-R1

Multi-channel Graphics Adapter Card for Reversed Lane Routing

2012-10-29

Preface

Copyright Notice

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Disclaimer

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Certification

MSC Technologies GmbH is certified according to DIN EN ISO 9001:2000 standards.

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Before contacting Technical Support of MSC Technologies GmbH, please consult the respective pages on our web site at www.msc-technologies.eu for the latest documentation, drivers and software downloads.

If the information provided there does not solve your problem, please contact our Technical Support:

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Content

1 General Information

1.1 Revision History

Rev.	Date	Description
0.1	2012-10-22	Draft
0.2	2012-10-29	1st released version
0.3	2014-09-09	Fixed Trade names

1.2 Reference Documents

[1] COM Express Module Base Specification
COM Express Revision 2.0
Last update: August 8th, 2010

[2] Digital Visual Interface DVI Revision 1.0
dvi_10.pdf
Last update: April 2nd, 1999
http://www.ddwg.org/

[3] High-Definition Multimedia Interface Specification Revision 1.3b
http://www.hdmi.org/

[4] VESA DisplayPort Standard Version 1, Revision 1a
DportV1.1a.pdf
Last update: January 11th, 2008
http://www.vesa.org/

2 Technical Description

2.1 Key features

The MSC CX-AD-DPHDMI-R1 is a multi-channel graphics adapter card that was developed for Type 2 COM Express Carrier boards that provide a PCIe x16 Graphics (PEG) slot with **reversed** lane routing between slot and COM Express connector. The card gives access to the digital display interfaces of Intel® 6 Series and Intel ® 7 Series chipsets on MSC CXB-6S and MSC CXB-6SI COM Express modules.

Key features include:

- Support for the digital display ports (DPB, DPC and DPD) of Intel® 6 Series and Intel® 7 Series Chipsets normally not available on COM Express Type 2.
- Plug-in compatible on standard COM Express Type 2 carrier boards with x16 PCIe (PEG) slots (reversal lane routing provided).
- Supports HDMI 1.3b, DVI 1.0 and DisplayPort 1.1a on each DDI port B[1)], C and D.
- Integrated TMDS level translators for HDMI and DVI.
- Adjustable DP voltage swing.
- Support for DVI monitors via HDMI to DVI cable adapter.
- Support for triple independent displays with MSC CXB-6SI modules (Intel ® 7 Series Chipsets) under Windows 7.

Note 1: Standard video BIOS supports SDVO on digital display port B.
In order to get support for HDMI, DVI and DP on digital display port B a customized BIOS version is needed. For more information please contact the MSC support (s. page 2).

2.2 Block diagram

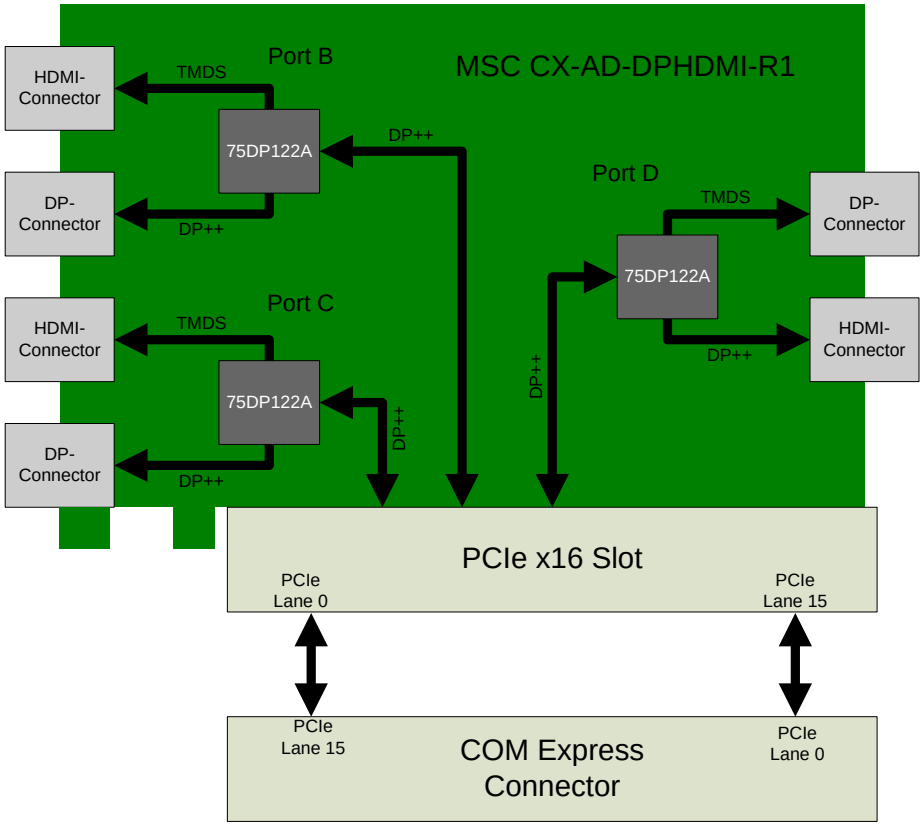


Fig. 1: MSC CX-AD-DPHDMI Block Diagram

2.3 Configuration

Each digital display port can be enabled or disabled and configured independently to support HDMI, DVI, or DisplayPort.

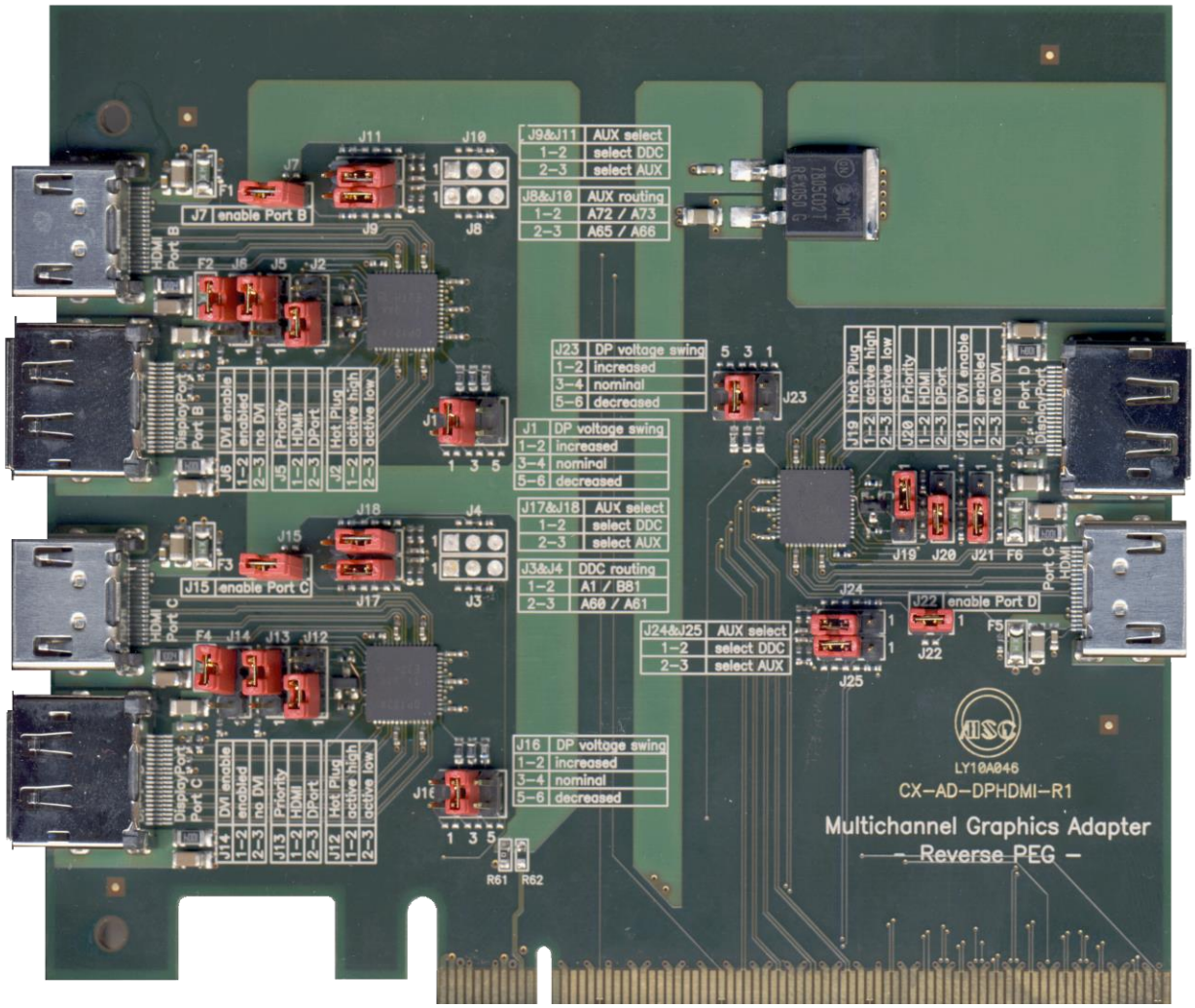


Fig. 2: Connectors and Jumpers

2.3.1 DDI Port enable

Port	Jumper	Open	Closed
B	J7	Disable	Enable
C	J15		
D	J22		

Closing a jumper connects a 2.2k pull-up resistor to the CTRLDATA signal of the appropriate chipset digital display port on the COM Express module. It operates as a functional strap, i.e. enabling or disabling an individual port requires a power off-on sequence.

In HDMI and DVI configuration the CTRLDATA line is used for panel communication. In DisplayPort configuration is serves as port enable strap only.

2.3.2 DP configuration

In order to configure a certain port to serve as DisplayPort (DP) the following jumper settings are necessary.

Port	Hot Plug	Priority	DVI enable	AUX select	
B	J2	J5	J6	J9	J11
C	J12	J13	J14	J17	J18
D	J19	J20	J21	J24	J25
Setting	1-2	2-3	2-3	2-3	2-3

In addition the DP lanes output voltage swing may be adjusted depending on the link quality between DP connector and DP monitor.

Port	DP voltage swing	1-2	3-4	5-6
B	J1	Increased voltage swing	Nominal voltage swing	Deceased voltage swing
C	J16			
D	J23			

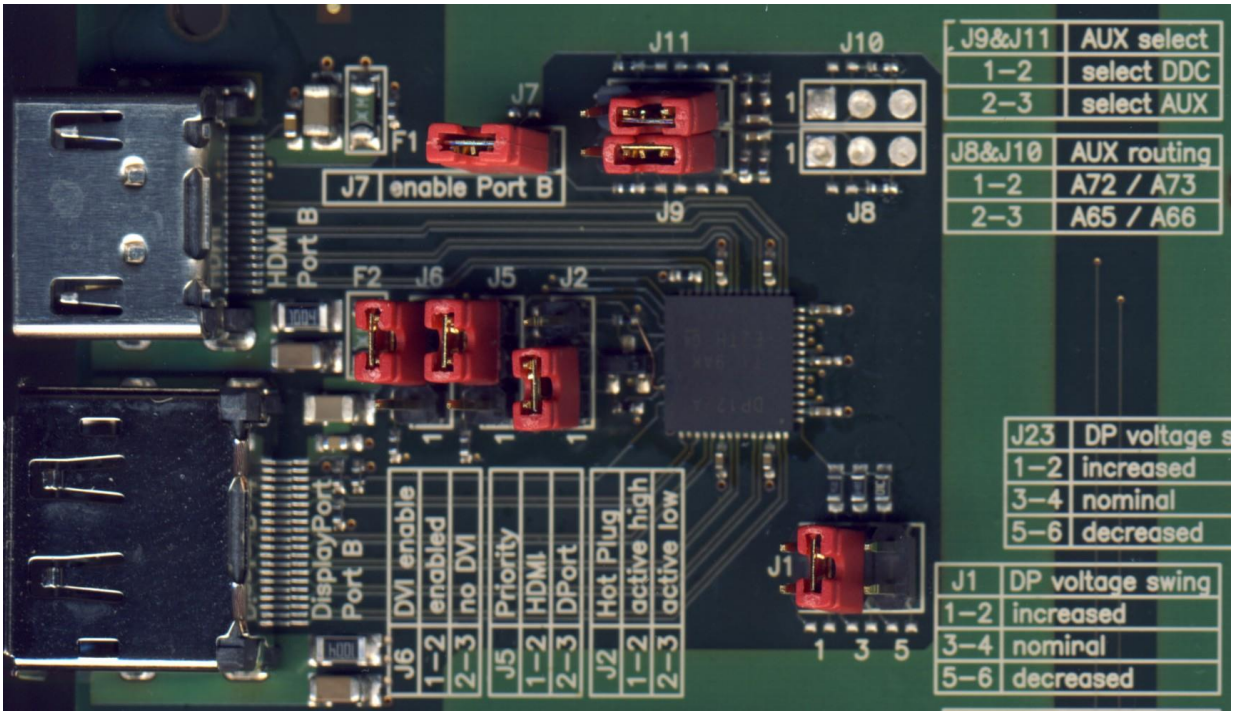


Fig. 3: Port B configured as DisplayPort using nominal voltage swing.

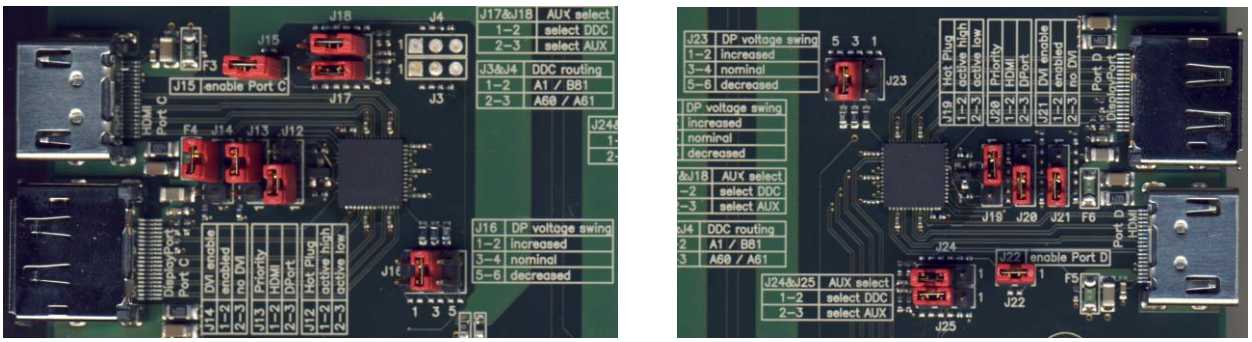


Fig. 4: Port C and port D configured as DisplayPort using nominal voltage swing.

2.3.3 DVI configuration

In order to configure a certain port to serve as Digital Visual Interface (DVI) the following jumper settings are necessary.

Port	Hot Plug	Priority	DVI enable	AUX select	
B	J2	J5	J6	J9	J11
C	J12	J13	J14	J17	J18
D	J19	J20	J21	J24	J25
Setting	1-2	1-2	1-2	1-2	1-2

Note: Jumper settings for DP voltage swing configuration have no effect in DVI mode.

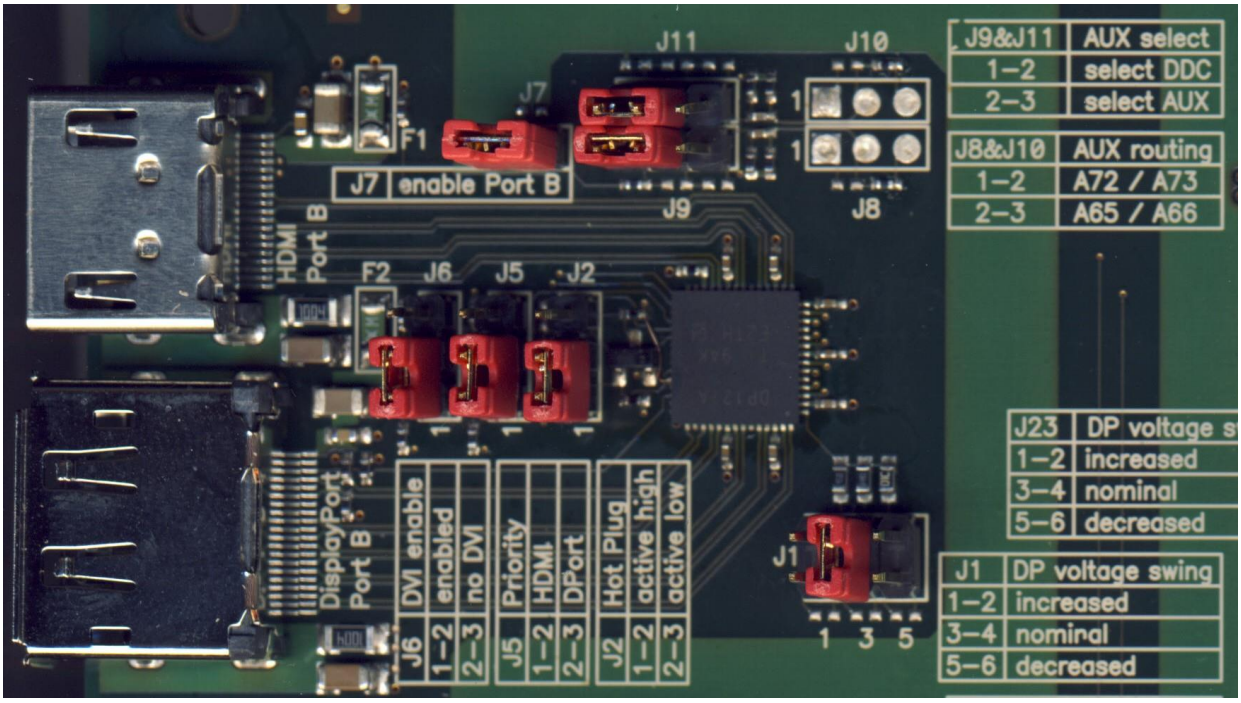
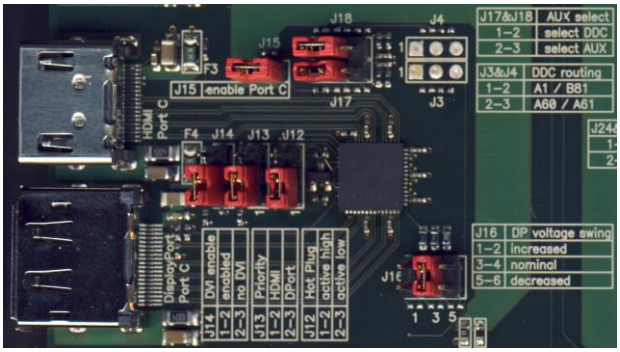


Fig. 5: Port B configured as DVI



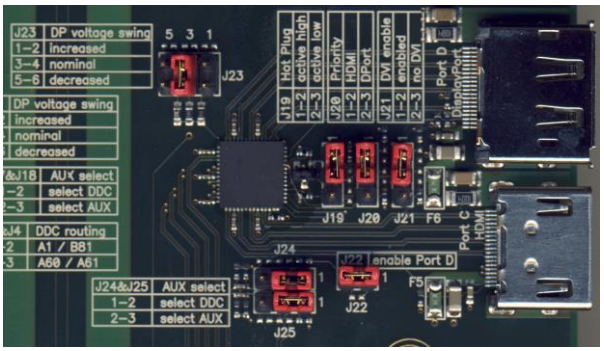


Fig. 6: Port C and port D configured as DVI

2.3.4 HDMI configuration

In order to configure a certain port to serve as High Definition Multimedia Interface (HDMI) the following jumper settings are necessary.

Port	Hot Plug	Priority	DVI enable	AUX select	
B	J2	J5	J6	J9	J11
C	J12	J13	J14	J17	J18
D	J19	J20	J21	J24	J25
Setting	1-2	1-2	2-3	1-2	1-2

Note: Jumper settings for DP voltage swing configuration have no effect in HDMI mode.

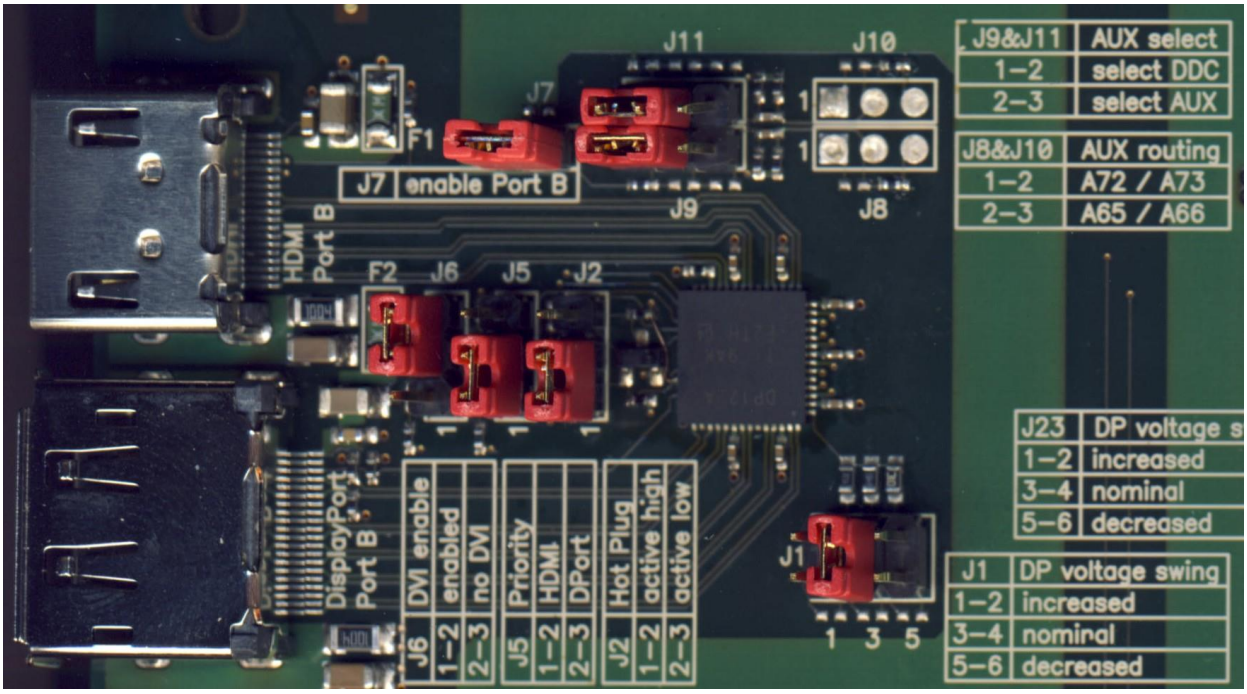


Fig. 7: Port B configured as HDMI

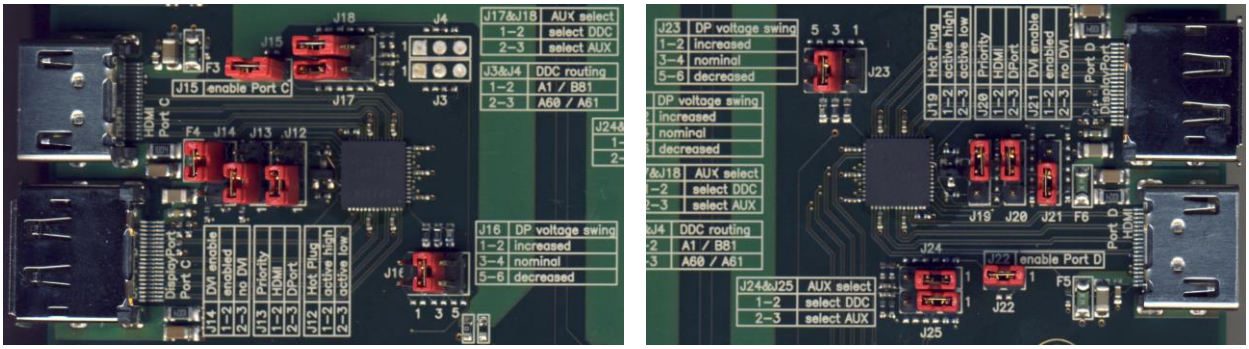


Fig. 8: Port C and port D configured as HDMI

2.4 Edge Finger Pin Assignment

COM Express Pin D54 PEG_LANE_RV# = 0 => reverse lane routing between COM Express connector and PCIe x16 slot							
COM Express Connector		**Edge Fingers** (PCIe x16 Slot)		COM Express pin D97 PEG_ENABLE# = 1			
				HDMI/DVI		**DisplayPort**	
Name	Pin	**Pin**	**Signal**	Signal	Description	Signal	Description
PEG_RX0+	C52	**A80**	**HSIp(15)**				
PEG_RX0-	C53	**A81**	**HSIn(15)**				
PEG_RX1+	C55	**A76**	**HSIp(14)**				
PEG_RX1-	C56	**A77**	**HSIn(14)**				
PEG_RX2+	C58	**A72**	**HSIp(13)**				
PEG_RX2-	C59	**A73**	**HSIn(13)**				
PEG_RX3+	C61	**A68**	**HSIp(12)**	TMDSB_HPD	HDMI Port B Hot Plug Detect	DPB_HPD	DisplayPort B Hot Plug Detect
PEG_RX3-	C62	**A69**	**HSIn(12)**				
PEG_RX4+	C65	**A64**	**HSIp(11)**			DPB_AUX+	DisplayPort B Auxiliary
PEG_RX4-	C66	**A65**	**HSIn(11)**			DPB_AUX-	Differential Pair
PEG_RX5+	C68	**A60**	**HSIp(10)**	TMDSC_CTRLCLK	HDMI Port C Control Clock (I^2C)		
PEG_RX5-	C69	**A61**	**HSIn(10)**	TMDSC_CTRLDATA [1)]	Port C Enable Strap HDMI Port C Control Data (I^2C)	DPC_ CTRLDATA [1)]	Port C Enable Strap
PEG_RX6+	C71	**A56**	**HSIp(9)**			DPC_AUX+	DisplayPort C Lane3 differential
PEG_RX6-	C72	**A57**	**HSIn(9)**			DPC_AUX-	Pair
PEG_RX7+	C74	**A52**	**HSIp(8)**	TMDSC_HPD	HDMI Port C Hot Plug Detect	DPC_HPD	DisplayPort C Hot Plug Detect
PEG_RX7-	C75	**A53**	**HSIn(8)**				
PEG_RX8+	C78	**A47**	**HSIp(7)**	TMDSD_CTRLCLK	HDMI Port D Control Clock (I^2C)		
PEG_RX8-	C79	**A48**	**HSIn(7)**	TMDSD_CTRLDATA [1)]	Port D Enable Strap HDMI Port D Control Data (I^2C)	DPD_ CTRLDATA [1)]	Port D Enable Strap
PEG_RX9+	C81	**A43**	**HSIp(6)**				
PEG_RX9-	C82	**A44**	**HSIn(6)**				
PEG_RX10+	C85	**A39**	**HSIp(5)**			DPD_AUX+	DisplayPort D Auxiliary
PEG_RX10-	C86	**A40**	**HSIn(5)**			DPD_AUX-	Differential Pair
PEG_RX11+	C88	**A35**	**HSIp(4)**	TMDSD_HPD	HDMI Port D Hot Plug Detect	DPD_HPD	DisplayPort D Hot Plug Detect
PEG_RX11-	C89	**A36**	**HSIn(4)**				
PEG_RX12+	C91	**A29**	**HSIp(3)**				
PEG_RX12-	C92	**A30**	**HSIn(3)**				
PEG_RX13+	C94	**A25**	**HSIp(2)**				
PEG_RX13-	C95	**A26**	**HSIn(2)**				
PEG_RX14+	C98	**A21**	**HSIp(1)**				
PEG_RX14-	C99	**A22**	**HSIn(1)**				
PEG_RX15+	C101	**A16**	**HSIp(0)**				
PEG_RX15-	C102	**A17**	**HSIn(0)**				

1) CTRLDATA pins do have strap functionality and are sampled during power up. A high level on these pins enables the appropriate Digital Display Interface Port B, C or D inside the PCH.

COM Express Pin D54 PEG_LANE_RV# = 0 => reverse lane routing between COM Express connector and PCIe x16 slot							
COM Express Connector		**Edge Fingers** (PCIe x16 Slot)		COM Express pin D97 PEG_ENABLE# = 1			
				HDMI/DVI		**DisplayPort**	
Name	Pin	**Pin**	**Signal**	Signal	Description	Signal	Description
PEG_TX0+	D52	**B78**	**HSOp(15)**	TMDSB_DATA2+	HDMI Port B Data 2 Differential	DPB_LANE0+	DisplayPort B Lane0
PEG_TX0-	D53	**B79**	**HSOn(15)**	TMDSB_DATA2-	Pair	DPB_LANE0-	differential Pair
SDVO_CTRLCLK	D73	**B17**	**PRSNT2#_B1**	TMDSB_CTRLCLK	HDMI Port B Control Clock (I^2C)		
PEG_TX1+	D55	**B74**	**HSOp(14)**	TMDSB_DATA1+	HDMI Port B Data 1 Differential	DPB_LANE1+	DisplayPort B Lane1
PEG_TX1-	D56	**B75**	**HSOn(14)**	TMDSB_DATA1-	Pair	DPB_LANE1-	differential Pair
PEG_TX2+	D58	**B70**	**HSOp(13)**	TMDSB_DATA0+	HDMI Port B Data 0 Differential	DPB_LANE2+	DisplayPort B Lane2
PEG_TX2-	D59	**B71**	**HSOn(13)**	TMDSB_DATA0-	Pair	DPB_LANE2-	differential Pair
PEG_TX3+	D61	**B66**	**HSOp(12)**	TMDSB_CK+	HDMI Port B Clock Differential Pair	DPB_LANE3+	DisplayPort B Lane3
PEG_TX3-	D62	**B67**	**HSOn(12)**	TMDSB_CK-		DPB_LANE3-	differential Pair
SDVO_CTRLDATA [1)]	C73	**B31**	**PRSNT2#_B2**	TMDSB_CTRLDATA [1)]	HDMI Port B Control Data (I^2C)	DPB_CTRLDATA [1)]	Refer to Note 1
PEG_TX4+	D65	**B62**	**HSOp(11)**	TMDSC_DATA2+	HDMI Port C Data 2 Differential	DPC_LANE0+	DisplayPort C Lane0
PEG_TX4-	D66	**B63**	**HSOn(11)**	TMDSC_DATA2-	Pair	DPC_LANE0-	differential Pair
PEG_TX5+	D68	**B58**	**HSOp(10)**	TMDSC_DATA1+	HDMI Port C Data 1 Differential	DPC_LANE1+	DisplayPort C Lane1
PEG_TX5-	D69	**B59**	**HSOn(10)**	TMDSC_DATA1-	Pair	DPC_LANE1-	differential Pair
PEG_TX6+	D71	**B54**	**HSOp(9)**	TMDSC_DATA0+	HDMI Port C Data 0 Differential	DPC_LANE2+	DisplayPort C Lane2
PEG_TX6-	D72	**B55**	**HSOn(9)**	TMDSC_DATA0-	Pair	DPC_LANE2-	differential Pair
PEG_TX7+	D74	**B50**	**HSOp(8)**	TMDSC_CK+	HDMI Port C Clock Differential Pair	DPC_LANE3+	DisplayPort C Lane3
PEG_TX7-	D75	**B51**	**HSOn(8)**	TMDSC_CK-		DPC_LANE3-	differential Pair
PEG_ENABLE#	D97	**B48**	**PRSNT2#_B3**				
PEG_TX8+	D78	**B45**	**HSOp(7)**	TMDSD_DATA2+	HDMI Port D Data 2 Differential	DPD_LANE0+	DisplayPort D Lane0
PEG_TX8-	D79	**B46**	**HSOn(7)**	TMDSD_DATA2-	Pair	DPD_LANE0-	differential Pair
PEG_TX9+	D81	**B41**	**HSOp(6)**	TMDSD_DATA1+	HDMI Port D Data 1 Differential	DPD_LANE1+	DisplayPort D Lane1
PEG_TX9-	D82	**B42**	**HSOn(6)**	TMDSD_DATA1-	Pair	DPD_LANE1-	differential Pair
PEG_TX10+	D85	**B37**	**HSOp(5)**	TMDSD_DATA0+	HDMI Port D Data 0 Differential	DPD_LANE2+	DisplayPort D Lane2
PEG_TX10-	D86	**B38**	**HSOn(5)**	TMDSD_DATA0-	Pair	DPD_LANE2-	differential Pair
PEG_TX11+	D88	**B33**	**HSOp(4)**	TMDSD_CK+	HDMI Port D Clock Differential Pair	DPD_LANE3+	DisplayPort D Lane3
PEG_TX11-	D89	**B34**	**HSOn(4)**	TMDSD_CK-		DPD_LANE3-	differential Pair
PEG_TX12+	D91	**B27**	**HSOp(3)**				
PEG_TX12-	D92	**B28**	**HSOn(3)**				
PEG_TX13+	D94	**B23**	**HSOp(2)**				
PEG_TX13-	D95	**B24**	**HSOn(2)**				
PEG_TX14+	D98	**B19**	**HSOp(1)**				
PEG_TX14-	D99	**B20**	**HSOn(1)**				
PEG_TX15+	D101	**B14**	**HSOp(0)**				
PEG_TX15-	D102	**B15**	**HSOn(0)**				
PEG_ENABLE#	D97	**B81**	**PRSNT2#_B4**				